ABSTRACT OF THE DISCLOSURE

A semiconductor device and its manufacturing method are provided in which the trade-off relation between channel resistance and JFET resistance, an obstacle to device miniaturization, is improved and the same mask is used to form a source region and a base region by ion implantation. In a vertical MOSFET that uses SiC, a source region and a base region are formed by ion implantation using the same tapered mask to give the base region a tapered shape. The taper angle of the tapered mask is set to 30° to 60° when the material of the tapered mask has the same range as SiC in ion implantation, and to 20° to 45° when the material of the tapered mask is SiO_2.